

# NTD5414N, NVD5414N

## Power MOSFET

### 24 A, 60 V Single N-Channel DPAK



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#### Features

- Low  $R_{DS(on)}$
- High Current Capability
- Avalanche Energy Specified
- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

#### Applications

- LED Lighting and LED Backlight Drivers
- DC-DC Converters
- DC Motor Drivers
- Power Supplies Secondary Side Synchronous Rectification

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX (Note 1)
60 V	37 mΩ @ 10 V	24 A

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ Unless otherwise specified)

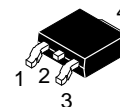
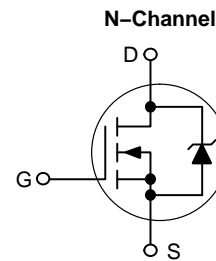
Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	60	V	
Gate-to-Source Voltage – Continuous		$V_{GS}$	$\pm 20$	V	
Gate-to-Source Voltage – Nonrepetitive ( $T_P < 10 \mu\text{s}$ )		$V_{GS}$	$\pm 30$	V	
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$	24	A
		$T_C = 100^\circ\text{C}$		16	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	$P_D$	55	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$		$I_{DM}$	75	A
Operating and Storage Temperature Range		$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)		$I_S$	24	A	
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 50 V_{dc}$ , $V_{GS} = 10 V$ , $I_L(pk) = 24 A$ , $L = 0.3 \text{ mH}$ , $R_G = 25 \Omega$ )		$E_{AS}$	86.4	mJ	
Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds		$T_L$	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE RATINGS

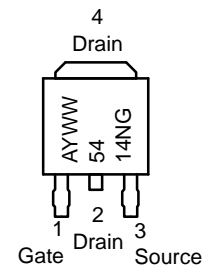
Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) Steady State (Note 1)	$R_{\theta JC}$	2.7	$^\circ\text{C}/\text{W}$
	$R_{\theta JA}$	58.6	

1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [1 oz] including traces).



**DPAK  
CASE 369AA  
STYLE 2**

#### MARKING DIAGRAMS & PIN ASSIGNMENT



- A = Assembly Location\*
- Y = Year
- WW = Work Week
- 5414N = Specific Device Code
- G = Pb-Free Device

\* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NTD5414N, NVD5414N

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C Unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>DS</sub> = 0 V, I <sub>D</sub> = 250 μA	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			67.3		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V V <sub>DS</sub> = 60 V	T <sub>J</sub> = 25°C		1.0	μA
			T <sub>J</sub> = 150°C		50	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA

## ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	2.0	3.2	4.0	V
Negative Threshold Temperature Coefficient	V <sub>GS(th)</sub> /T <sub>J</sub>			0.74		mV/°C
Drain-to-Source On-Voltage	V <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 24 A		0.7	1.16	V
			V <sub>GS</sub> = 10 V, I <sub>D</sub> = 12 A, 150°C		0.7	
Drain-to-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 24 A		28.4	37	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A		24		S

## CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz		800	1200	pF
Output Capacitance	C <sub>oss</sub>			165		
Transfer Capacitance	C <sub>rss</sub>			75		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 48 V, I <sub>D</sub> = 24 A		25	48	nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			1.1		
Gate-to-Source Charge	Q <sub>GS</sub>			4.8		
Gate-to-Drain Charge	Q <sub>GD</sub>			11.3		

## SWITCHING CHARACTERISTICS, V<sub>GS</sub> = 10 V (Note 3)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 48 V, I <sub>D</sub> = 24 A, R <sub>G</sub> = 9.1 Ω		12		ns
Rise Time	t <sub>r</sub>			58		
Turn-Off Delay Time	t <sub>d(off)</sub>			47		
Fall Time	t <sub>f</sub>			69		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage (Note 2)	V <sub>SD</sub>	V <sub>GS</sub> = 0 V I <sub>S</sub> = 24 A	T <sub>J</sub> = 25°C	0.92	1.15	V
			T <sub>J</sub> = 125°C	0.8		
Reverse Recovery Time	t <sub>rr</sub>	I <sub>S</sub> = 24 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> , dI <sub>S</sub> /dt = 100 A/μs		45.7		ns
Charge Time	t <sub>a</sub>			31.7		
Discharge Time	t <sub>b</sub>			14		
Reverse Recovery Stored Charge	Q <sub>RR</sub>			76		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3. Switching characteristics are independent of operating junction temperatures.

# NTD5414N, NVD5414N

## TYPICAL PERFORMANCE CURVES

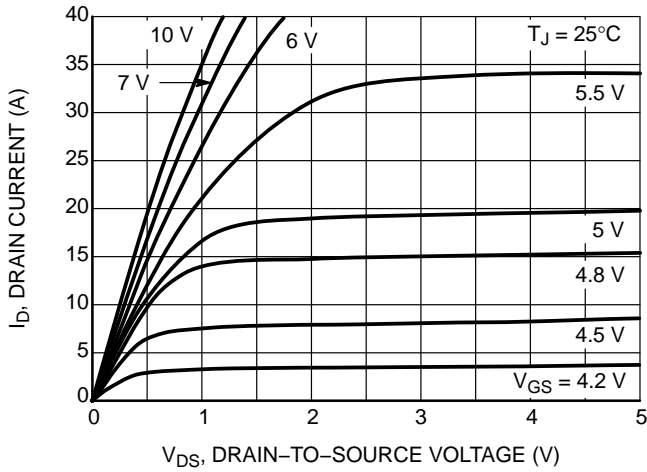


Figure 1. On-Region Characteristics

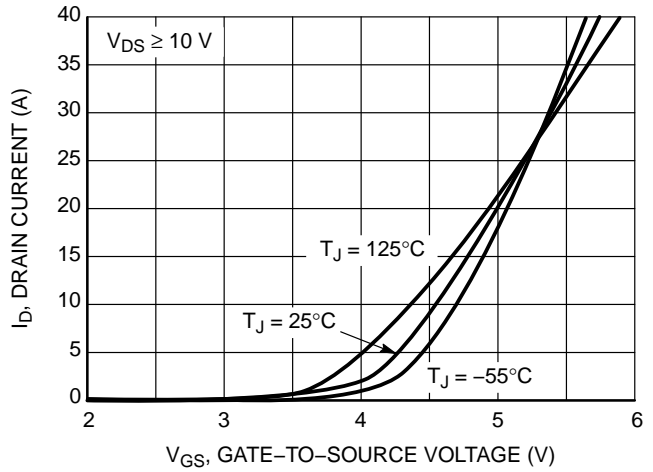


Figure 2. Transfer Characteristics

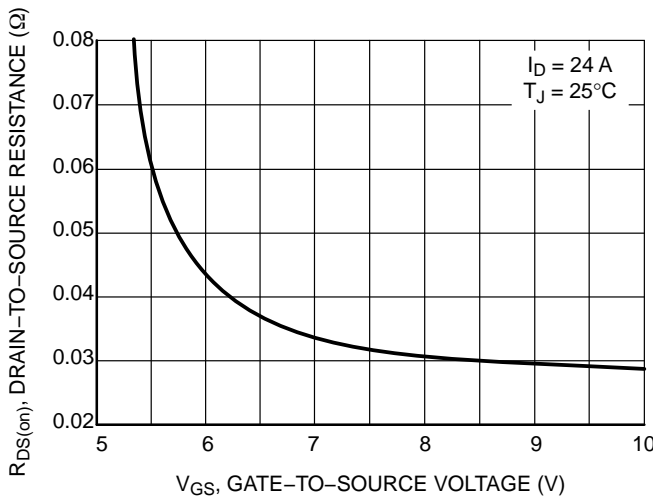


Figure 3. On-Resistance vs. Gate-to-Source Voltage

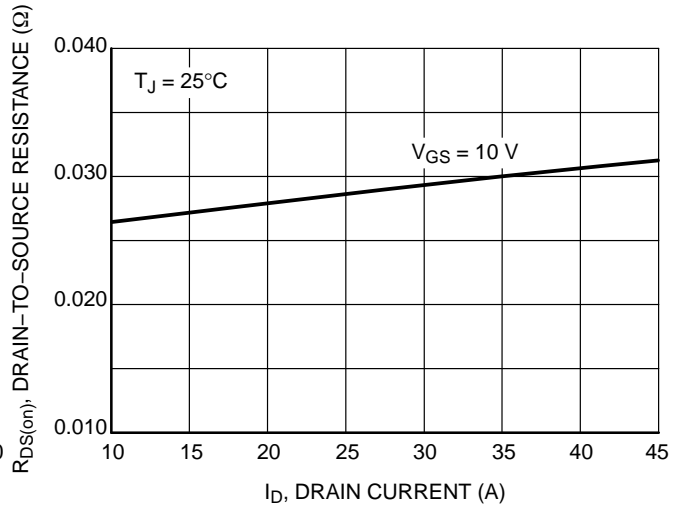


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

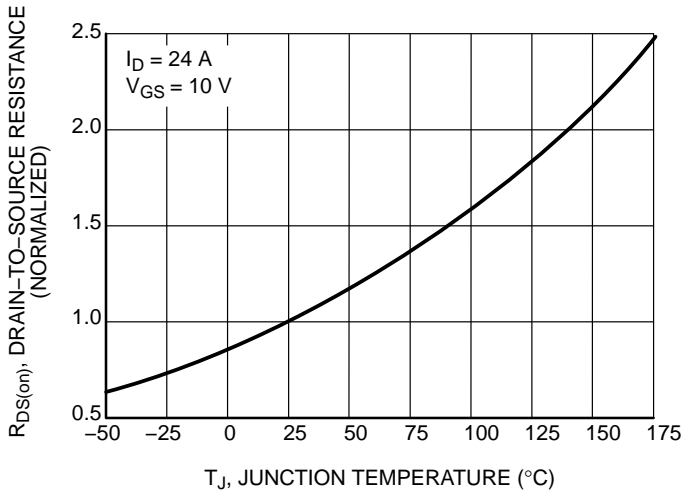


Figure 5. On-Resistance Variation with Temperature

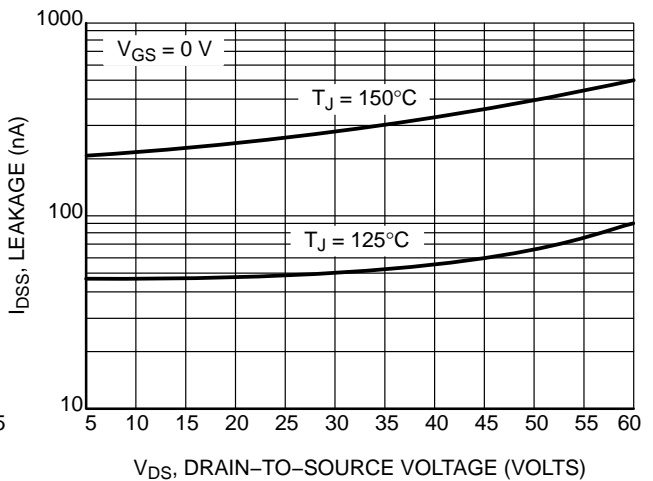


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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## TYPICAL PERFORMANCE CURVES

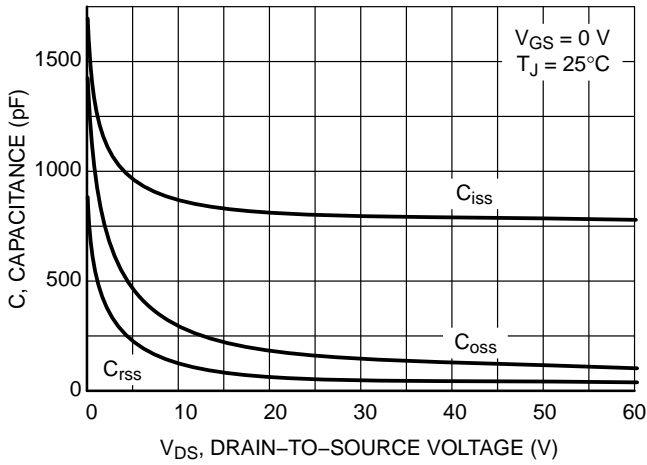


Figure 7. Capacitance Variation

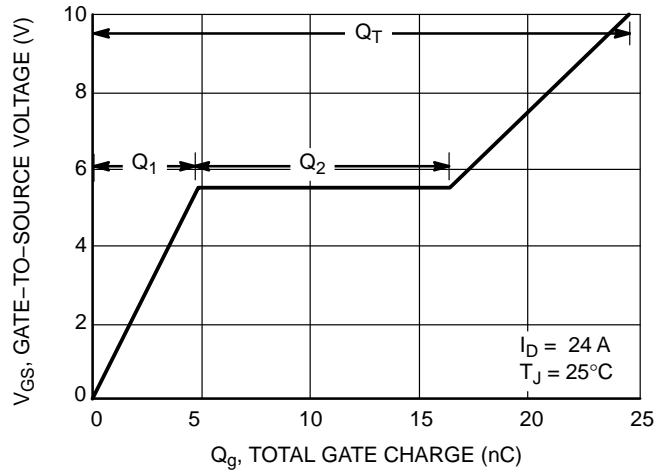


Figure 8. Gate-to-Source Voltage vs. Total Charge

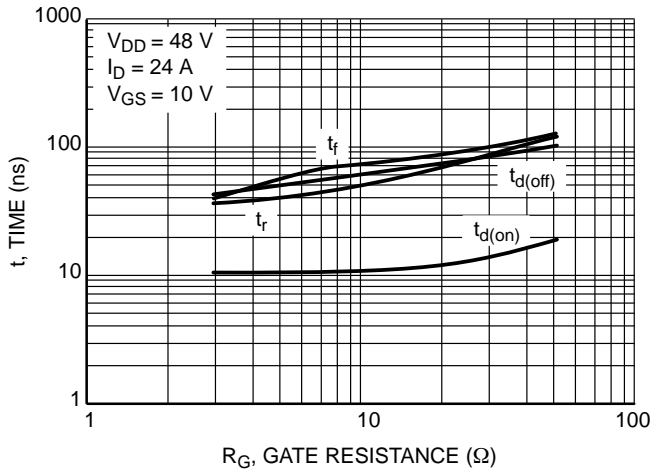


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

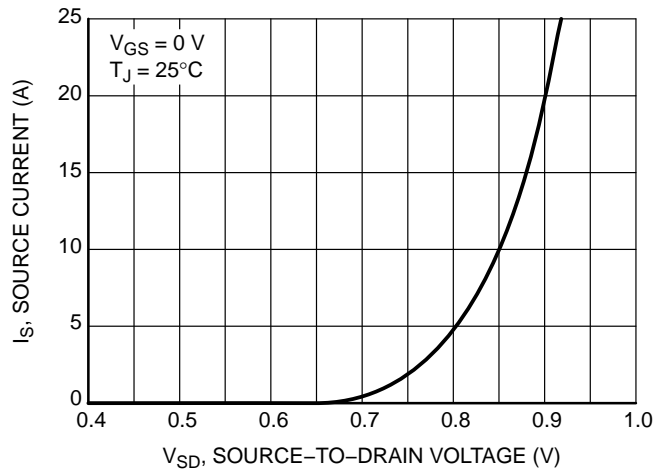


Figure 10. Diode Forward Voltage vs. Current

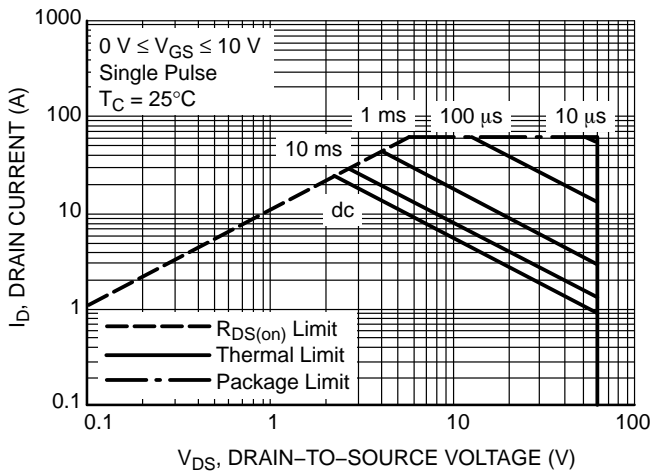


Figure 11. Maximum Rated Forward Biased Safe Operating Area

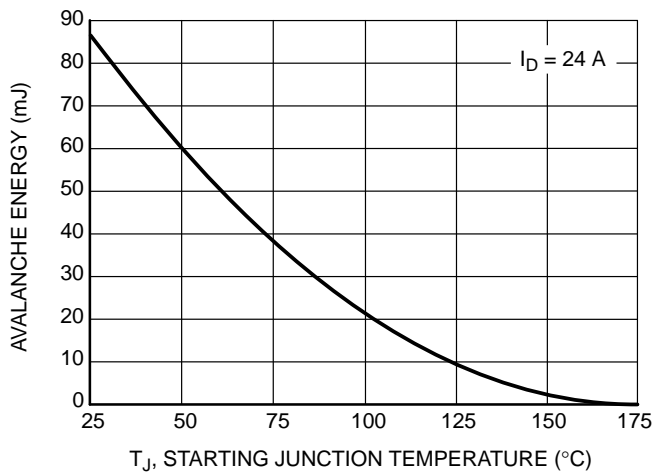


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

# NTD5414N, NVD5414N

## TYPICAL PERFORMANCE CURVES

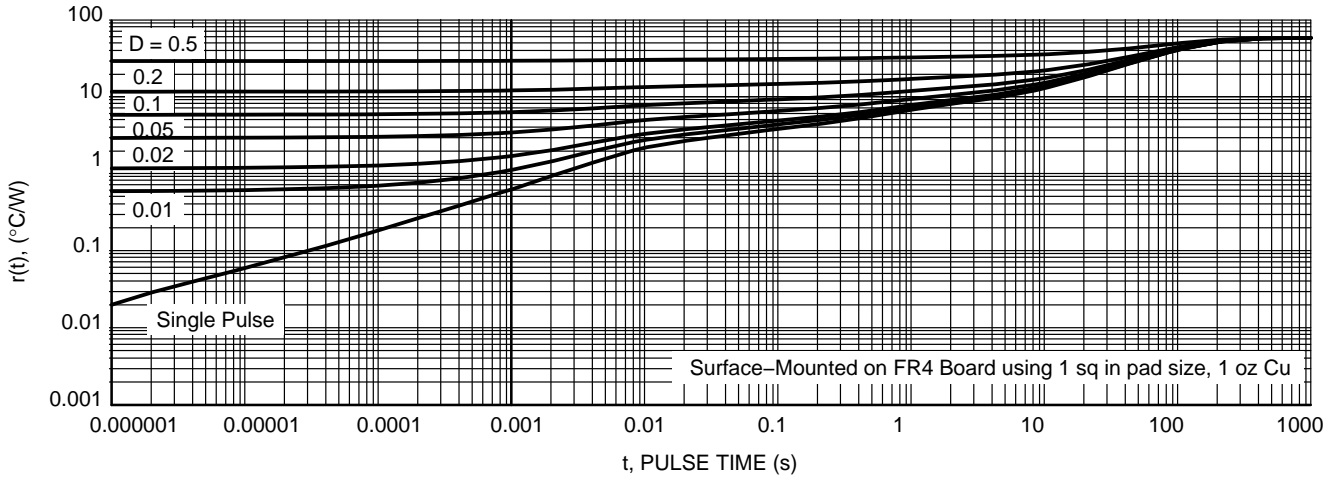


Figure 13. Thermal Response

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTD5414NT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NVD5414NT4G*	DPAK (Pb-Free)	2500 / Tape & Reel

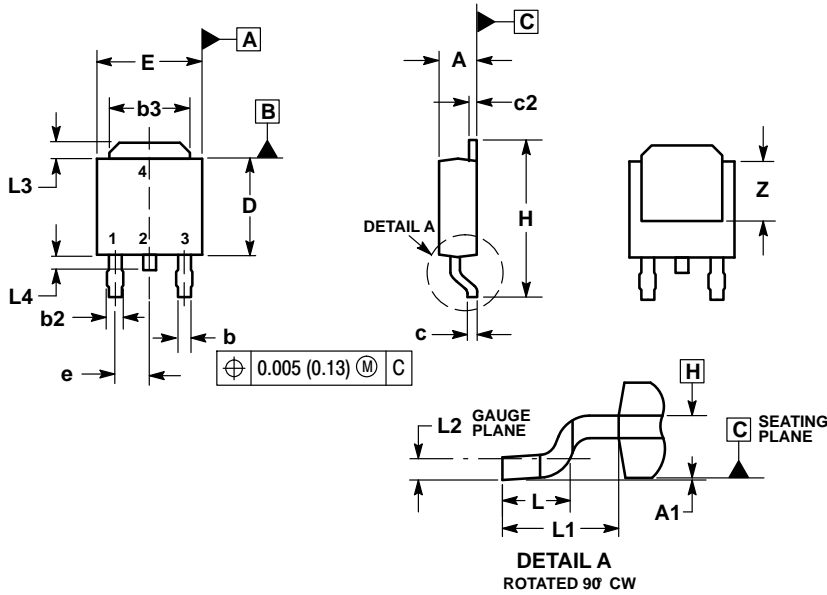
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

# NTD5414N, NVD5414N

## PACKAGE DIMENSIONS

### DPAK (SINGLE GAUGE) CASE 369AA ISSUE B

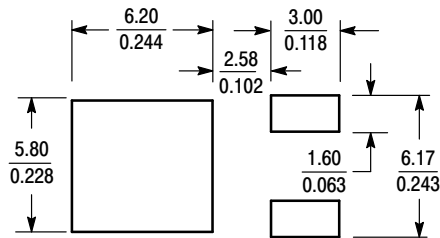


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

### SOLDERING FOOTPRINT\*




SCALE 3:1  $\left(\frac{\text{mm}}{\text{inches}}\right)$

#### STYLE 2:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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