



## Test Procedure for the NCV47411PAAJGEVB Evaluation Board

The NCV47411 is dual channel adjustable Low Dropout Regulator with:

- Two adjustable output voltages from 3.3 V to 20 V
- Two adjustable current limits up to 150 mA
- Enable inputs with 3.3 V Logic compatible thresholds

Power supplying of the chip is possible from one or two independent sources. **INPUT1** must be always supplied and **INPUT2** as optional for  $V_{in2}$  supply.

### 1. Power supplying

#### a. Power supplying from one source

Connect the test setup as is shown in **Figure 1** (See **Table 1** with required equipment). Connect power supply to **INPUT1** connector **J<sub>1</sub>** (Power supplying of **INPUT2** is not needed).

- **Hi\_F** – Positive Force line
- **Hi\_S** – Positive Sense line
- **Lo\_F** – Negative Force line
- **Lo\_S** – Negative Sense line

Connect  $V_{in2}$  pin to **INPUT1** via appropriate position of jumper “ **$V_{in2}$  to IN1 or IN2 connection**”.

#### b. Power supplying from two sources

Connect the test setup as is shown in **Figure 1** (See **Table 1** with required equipment). Connect two power supplies to **INPUT1** connector **J<sub>1</sub>** and to **INPUT2** connector **J<sub>2</sub>**, respectively.

- **Hi\_F** – Positive Force line
- **Hi\_S** – Positive Sense line
- **Lo\_F** – Negative Force line
- **Lo\_S** – Negative Sense line

Values of input voltages  $V_{in1}$  and  $V_{in2}$  can be different. This option is suitable for reducing of power dissipation on chip.

Connect  $V_{in2}$  pin to **INPUT2** via appropriate position of jumper “ **$V_{in2}$  to IN1 or IN2 connection**”.

### 2. Connect jumpers **J<sub>10</sub> – J<sub>13</sub>** for output current limitation from $V_{out1}$ pin and **J<sub>20</sub> – J<sub>23</sub>** for output current limitation from $V_{out2}$ pin.

- **J<sub>n0</sub>** –  $I_{LIMn0} \sim 10$  mA
- **J<sub>n1</sub>** –  $I_{LIMn1} \sim 50$  mA
- **J<sub>n2</sub>** –  $I_{LIMn2} \sim 100$  mA
- **J<sub>n3</sub>** –  $I_{LIMn3} - R_{CSOn3}$  positions available for individual current limit setting by resistor from range 850  $\Omega$  to 12.75 k $\Omega$

### 3. Set Input Voltage and turn on Power Supply/Supplies.

### 4. Enable output of the channel to power the regulated output voltage by connecting the **ENABLE** pin to corresponding $V_{in}$ via jumper. Enabling can be performed by external voltage source as well.

### 5. Load the outputs by resistive loads connected via jumpers:

- **J<sub>5</sub>, J<sub>7</sub>** – 51  $\Omega$
- **J<sub>6</sub>, J<sub>8</sub>** – 1 k $\Omega$

External loads can be used instead build-in resistive loads as well.

6. Monitor Output Voltages, given according to Equation 1.

$$V_{out\_nom\_n} = 1.275 \left( 1 + \frac{R_{n1}}{R_{n2}} \right) \quad (\text{eq. 1})$$

7. Monitor Current Sense Output voltages on appropriate connector. They should be max 2.55 V in steady state. The CSO voltages are proportional to output currents according to Equation 2.

$$V_{CSO\_n} = I_{out\_n} \left( R_{CSO\_n} \times \frac{1}{50} \right) \quad (\text{eq. 2})$$

8. Compare your results with measured results in **Table 2**.

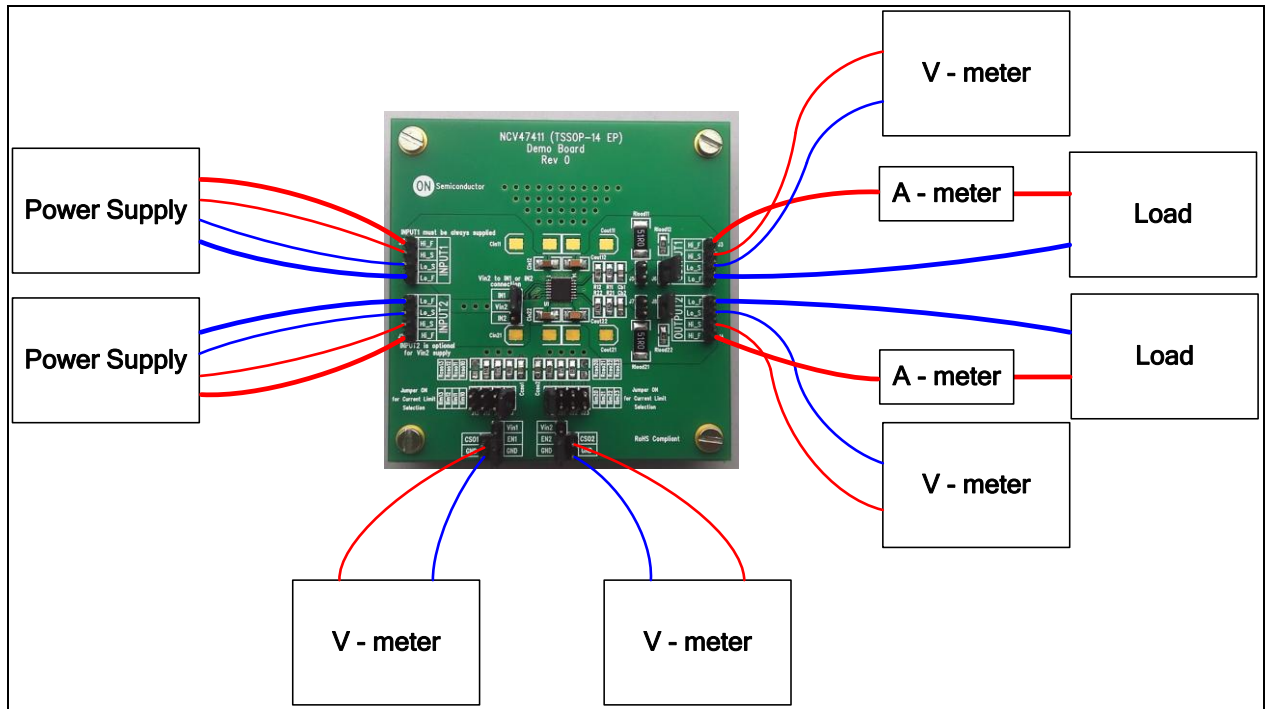


Figure 1. General Test Setup

Table 1: Required Equipment

Equipment	Ranges
Power Supply	0 V – 45 V / 1 A
Load	0 mA – 500 mA
V - meter	0 V – 20 V
A - meter	0 mA – 500 mA

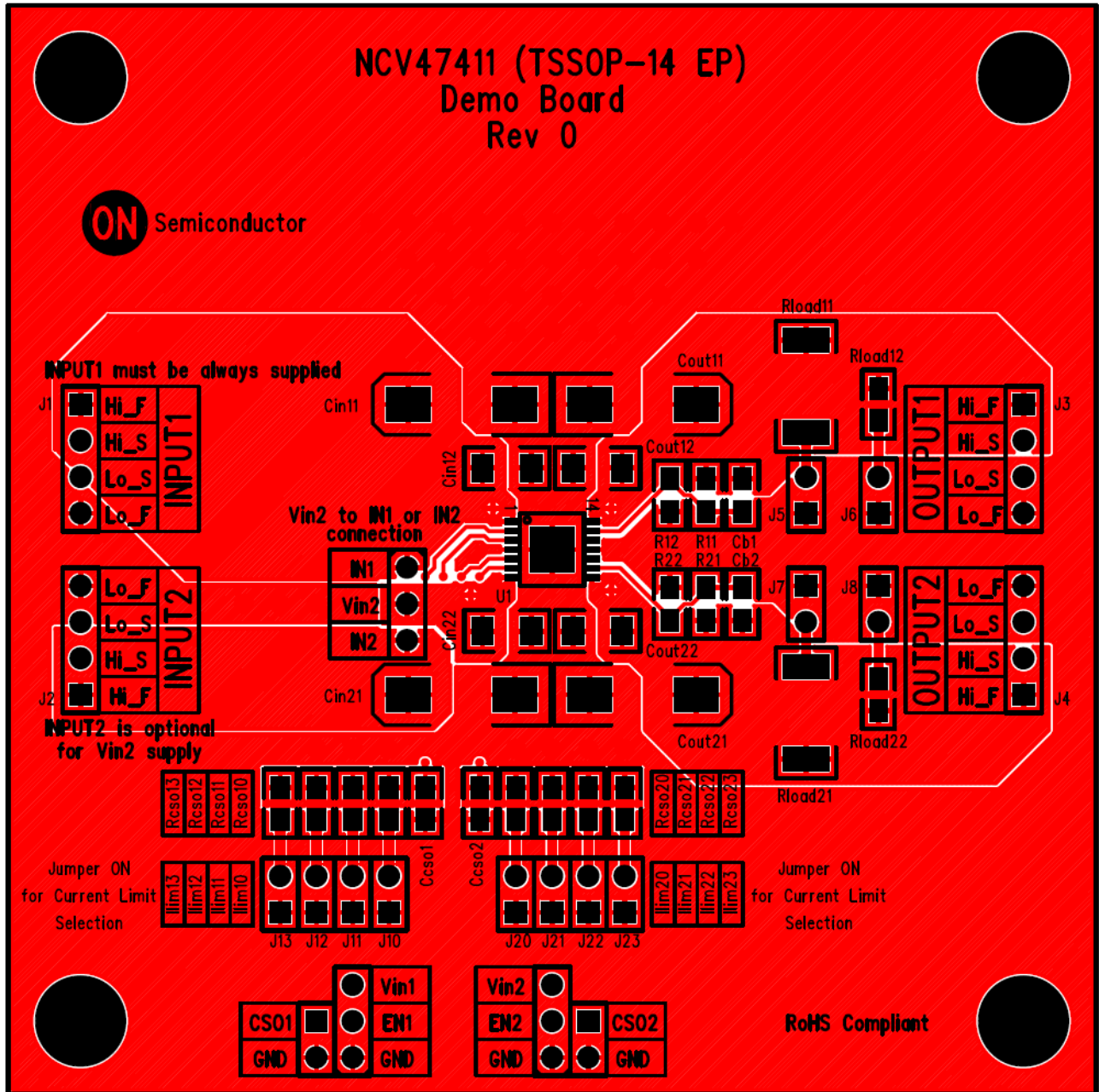


Figure 2. Top side PCB Layout (3 x 3 inch)

**Table 2: Measured Results**

Parameter	Test Conditions	Symbol	Value		Unit
			Nominal	Measured	
Output Voltage	$V_{in} = 13.5 \text{ V}, V_{out\_nom\_n} = 5.02 \text{ V}, I_{out\_n} = 5 \text{ mA}, R_{CSO\_n} = \text{Short to ground}$	$V_{out1}$	5.02	5.006	V
		$V_{out2}$		5.005	
	$V_{in} = 13.5 \text{ V}, V_{out\_nom\_n} = 5.02 \text{ V}, I_{out\_n} = 100 \text{ mA}, R_{CSO\_n} = \text{Short to ground}$	$V_{out1}$		5.005	
		$V_{out2}$		5.005	
Output Current	$V_{in} = 13.5 \text{ V}, V_{out\_nom\_n} = 5.02 \text{ V}, V_{out\_n} = 90 \% \text{ of } V_{out\_nom\_n}, R_{CSO\_n} = 12.7 \text{ k}\Omega$	$I_{out1}$	10.04	10.06	mA
		$I_{out2}$		10	
	$V_{in} = 13.5 \text{ V}, V_{out\_nom\_n} = 5.02 \text{ V}, V_{out\_n} = 90 \% \text{ of } V_{out\_nom\_n}, R_{CSO\_n} = 2.49 \text{ k}\Omega$	$I_{out1}$	51.2	52.47	
		$I_{out2}$		52.19	
	$V_{in} = 13.5 \text{ V}, V_{out\_nom\_n} = 5.02 \text{ V}, V_{out\_n} = 90 \% \text{ of } V_{out\_nom\_n}, R_{CSO\_n} = 1.2 \text{ k}\Omega$	$I_{out1}$	106.25	110.28	
		$I_{out2}$		109.95	
Output Current	$V_{in} = 13.5 \text{ V}, V_{out\_nom\_n} = 5.02 \text{ V}, V_{out\_n} = 0 \text{ V}, R_{CSO\_n} = 12.7 \text{ k}\Omega$	$I_{out1}$	10.04	10.55	mA
		$I_{out2}$		10.49	
	$V_{in} = 13.5 \text{ V}, V_{out\_nom\_n} = 5.02 \text{ V}, V_{out\_n} = 0 \text{ V}, R_{CSO\_n} = 2.49 \text{ k}\Omega$	$I_{out1}$	51.2	54.44	
		$I_{out2}$		54.17	
	$V_{in} = 13.5 \text{ V}, V_{out\_nom\_n} = 5.02 \text{ V}, V_{out\_n} = 0 \text{ V}, R_{CSO\_n} = 1.2 \text{ k}\Omega$	$I_{out1}$	106.25	115.32	
		$I_{out2}$		114.37	