PIC24F16KA102 Family Silicon Errata and Data Sheet Clarification

The PIC24F16KA102 family devices that you have received conform functionally to the current Device Data Sheet (DS39927**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24F16KA102 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**B1**).

Data Sheet clarifications and corrections start on Page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24F16KA102 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)				
		A5	A6	A7	B0	B1
PIC24F08KA101	0D08h	05h	06h	07h	08h	09h
PIC24F08KA102	0D0Ah					
PIC24F16KA101	0D01h					
PIC24F16KA102	0D03h					

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory. They are shown in hexadecimal in the format, "DEVID DEVREV".

2: Refer to the *"PIC24FXXKA1XX/FVXXKA3XX Family Flash Programming Specifications"* (DS39919) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]				
				A5	A6	A7	B0	B1
CTMU	—	1.	Module operates in Sleep mode.	X	X	X		
Resets	BOR	2.	Inadvertent Reset when disabling/enabling BOR.	X	X	X	X	X
Core	ICSP™	3.	Unable to use PGC/PGD pair under certain conditions.	X				
Core	Deep Sleep	4.	Failure to avoid Deep Sleep entry.	X	X	X		
Memory	Code Protection	5.	No direct jump to Boot Segment from Reset vector.	X				
Comparator	—	6.	Change in maximum VIOFF.	X	X	X		
SPI	Enhanced Buffer mode	7.	Errors when polling SPITBF flag.	X	X	X		
I/O Ports	PORTA and PORTB	8.	Under certain conditions, functionality for RB0 and RA0 pins does not work correctly.	X	X	X		
I/O Ports	PORTA and PORTB	9.	Under certain conditions, functionality for RB2 does not work correctly.	X	X	X		
Core	Low-Voltage BOR	10.	LPBOR configuration results in ambiguous Resets.	X	X	X		
Comparator	—	11.	Output polarity inversion also inverts edge-detect sensing.	X	X	X	X	X
Core	Doze mode	12.	Instruction execution glitches following DOZE bit changes.	X	X	X		
A/D Converter	—	13.	Module continues to draw current when disabled.	X	X	X		
HLVD	Band Gap Reference	14.	BGVST and IRVST bits may not become set at extremely low temperatures.	X	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B1**).

1. Module: CTMU

The CTMU and its current source may continue to operate in Sleep mode. This results in current consumption in excess of the specifications for Sleep.

Work around

Clear the CTMU Enable bit, CTMUEN (CTMUCON<15>), prior to entering Sleep mode.

Affected Silicon Revisions

A5	A6	A7	B0	B1			
X	X	X					

2. Module: Resets (BOR)

A device Reset may occur if the BOR is disabled and immediately re-enabled in software (RCON<14> is cleared and then immediately set).

Work around

It is recommended that several NOP instructions be added to a BOR disable/enable sequence. Alternatively, place several instructions or a short routine between the instructions to disable and enable the BOR.

Affected Silicon Revisions

A5	A6	A7	B0	B1			
X	X	X	X	X			

3. Module: Core (ICSP™)

Under certain circumstances, a PGCx/PGDx pin pair may not function to enter ICSP Programming mode. This has been observed only when both the following conditions are met:

c) Pin, RA5, is configured as $\overline{\text{MCLR}}$ (FPOR<5> = 1), and

d) The pins of the PGCx/PGDx pair were configured as digital outputs (corresponding TRISx bit cleared) in software.

In these circumstances, the pins do not switch to a high-impedance state upon entry into Programming mode, but remain configured as outputs.

Work around

Choose a PGCx/PGDx pair with pins that are always configured as inputs (TRISx bits are set).

Affected Silicon Revisions

A5	A6	A7	B0	B1			
X							

4. Module: Core (Deep Sleep)

Deep Sleep wake-up sources may be ignored if they occur just prior to entry into Deep Sleep mode. As a result, the device may enter Deep Sleep mode when it should not.

Work around

If possible, configure external Deep Sleep wake-up sources to repeat themselves once. If the device does enter Deep Sleep, the second occurrence of the wake-up source will wake the device.

Alternatively, synchronize the entry into Deep Sleep with external wake-up sources, where possible.

Affected Silicon Revisions

A5	A6	A7	B0	B1			
X	X	X					

5. Module: Memory (Code Protection)

When any Boot Segment is enabled in program memory (FBS<3:1> ≠ 111), it is not possible to jump directly from the Reset vector to any address in the Boot Segment.

Work around

Point the Reset vector to an address in the General Segment. From there, it is possible to jump into the Boot Segment.

Affected Silicon Revisions

A5	A6	A7	B0	B1			
X							

6. Module: Comparator

The maximum value for the input offset voltage (Parameter D300, VIOFF), shown in Table 29-13 of the device data sheet, has changed for this silicon revision. The new value is shown in Table 3 (changes in **bold**).

Work around

None.

Affected Silicon Revisions

A5	A6	A7	B0	B1			
X	X	X					

7. Module: SPI (Enhanced Buffer Mode)

In Enhanced Buffer mode (SPI1CON2<0> = 1), polling the SPI Transmit Buffer Full bit, SPITBF (SPI1STAT<1>), may produce erroneous results. This occurs only under two circumstances:

a) In Master mode, when the SPI divide clock is 4 or greater.

b) In Slave mode, when the SPI sample clock is slower than 1/4 of the CPU instruction time (TCY).

For Master mode, this includes all combinations of the primary prescale bits (SPI1CON1<1:0>) and secondary prescale bits (SPI1CON1<4:2>) that, when combined, create an SPI sample clock divisor with a value of four or greater.

Work around

Instead of polling the SPITBF bit to test for an empty buffer (SPI1STAT<1> = 0), implement a SPI receive interrupt handler in software and add to the SPI transmit buffer in this routine.

Alternatively, poll the SPI Receive Full bit, SPIRBF (SPI1STAT<0>), or the Shift Register Empty bit, SRMPT (SPI1STAT<7>), to determine when to service the SPI transmit and transmit buffers.

Affected Silicon Revisions

A5	A6	A7	B0	B1			
X	X	X					

TABLE 3: COMPARATOR DC SPECIFICATIONS (PARTIAL)

Param No.	Symbol	Characteristics	Min	Typ	Max	Units	Comments
	VIOFF	Input Offset Voltage	—	20	**60**	mV	

8. Module: I/O Ports (PORTA and PORTB)

The functions associated with port pins, RB0 and RA0, may be interconnected in unexpected ways.

PORTB pin, RB0, may not operate correctly as an input if the SPI module is enabled (SPI1CON<15> = 1). Additionally, the pull-up, pull-down and the Change Notification (CN4) functionality are disabled. RB0 does operate correctly with the SPI enabled if it is configured as an output.

PORTA pin, RA0, may not operate correctly as an input when the open-drain output is enabled for RB0 (ODCB<0>). RA0 will operate correctly as an output.

However, when the analog input on RB0 (AN2) is enabled (AD1PCFG<2> = 0) and the SPI module is enabled, RB0 will be driven as a digital output, not as a analog input.

Work around

To enable RB0 as a digital input, enable the open-drain output for RB0 (ODCB<0>) and set the latch bit (LATB<0> = 1). The Change Notification (CN4), pull-up and pull-down for this pin will function correctly as well.

This work around may cause RA0 to function incorrectly. There is no known work around for RA0 as an input and RB0 with the open-drain output enabled.

To enable RB0 as an analog input when SPI is enabled:

1. Enable the open-drain output for RB0 (ODCB<0>).
2. Set the latch bit (LATB<0> = 1).
3. Clear TRISB<0>.
4. Clear AD1PCFG<2>.

Affected Silicon Revisions

A5	A6	A7	B0	B1			
X	X	X					

9. Module: I/O Ports (PORTA and PORTB)

Note: This issue occurs in PIC24FXXKA101 (20-pin) devices only.

On 20-pin devices of the PIC24F16KA102 family, the functions associated with port pins, RB2 and RA2, may be interconnected in unexpected ways.

PORTB pin, RB2, may not operate correctly as a digital I/O if the analog input on PORTA pin, RA2 (AN4), is enabled (AD1PCFG<4> = 0). Both the digital port and the U1RX functionality, multiplexed to RB2, are disabled.

Although this issue is similar in form to Silicon Issue 8, it appears to be independent in its root cause.

Work around

None.

Affected Silicon Revisions

A5	A6	A7	B0	B1			
X	X	X					

10. Module: Core (Low-Power BOR)

When the Low-Power BOR (LPBOR) is enabled (FPOR<6:5> = 00), BOR events may result in a device Reset, in which both the BOR and POR bits are set.

This differs from the expected behavior of simply re-arming the POR circuit to ensure that a POR occurs when V_{DD} drops below the POR threshold.

Work around

None.

Affected Silicon Revisions

A5	A6	A7	B0	B1			
X	X	X					

11. Module: Comparator

When a comparator is programmed to trigger on certain edge-detect events (CMxCON<7:6> = 10 or 01), setting the CPOL bit (CMxCON<13> = 1) may cause the comparator to flag the opposite edge-detect event (e.g., a high-to-low edge instead of the programmed low-to-high).

Work around

Leave CPOL = 0.

Affected Silicon Revisions

A5	A6	A7	B0	B1			
X	X	X	X	X			

12. Module: Core (Doze Mode)

Operations that immediately follow any manipulations of the DOZE<2:0> or DOZEN bits (CLKDIV<14:11>) may not execute properly. In particular, for instructions that operate on an SFR, data may not be read properly. Also, bits automatically cleared in hardware may not be cleared if the operation occurs during this interval.

Work around

Always insert a NOP instruction before and after either of the following:

- Enabling or disabling Doze mode by setting or clearing the DOZEN bit
- Before or after changing the DOZE<2:0> bits

Affected Silicon Revisions

A5	A6	A7	B0	B1			
X	X	X					

13. Module: A/D Converter

Once the A/D module is enabled (AD1CON1<15> = 1), it may continue to draw extra current even if the module is later disabled (AD1CON1<15> = 0).

Work around

In addition to disabling the module through the ADON bit, set the corresponding PMD bit (ADC1MD, PMD1<0>) to power it down completely.

Disabling the A/D module through the PMD1 register also disables the AD1PCFG registers, which in turn, affects the state of any port pins with analog inputs. Users should consider the effect on I/O ports and other digital peripherals on those ports when ADC1MD is used for power conservation.

Affected Silicon Revisions

A5	A6	A7	B0	B1			
X	X	X					

14. Module: HLVD (Band Gap Reference)

At the extreme low end of the operating temperature range (near -40°C), the BGVST and IRVST flag bits (HLVDCON<6:5>) may not become set when the voltage references are stable and ready to use.

Work around

For applications that run at extremely cold temperatures, do not use the BGVST and IRVST bits as the sole indicator of band gap readiness. Include a time-out of 750 µs between enabling and using a reference.

Affected Silicon Revisions

A5	A6	A7	B0	B1			
X	X	X	X	X			

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the Device Data Sheet (DS39927**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Memory

In Table 4-4, the CN9IE, CN9PUE and CN9PDE bits (CNEN1<9>, CNPU1<9> and CNPD1<9>, respectively) are not implemented on 20-pin devices. These bits are to be marked with the existing Footnote 1 (“These bits are not implemented in 20-pin devices”).

2. Module: A/D

In Register 22-3, the values shown for AD1CON3<5:0> (ADCS<5:0>) are incorrect. The corrected values are shown below (changes in bold).

REGISTER 22-3: AD1CON3: A/D CONTROL REGISTER 3

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC	—	—	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 5-0 ADCS<5:0>: A/D Conversion Clock Select bits

111111 = 64 • TCY
111110 = 63 • TCY
.
.
.
000001 = 2 • TCY
000000 = TCY

3. Module: Electrical Specifications (DC Specification)

Table 29-5 (“BOR Trip Points”) has changed to reflect the functionality of the LPBOR trip point (BORV<1:0> = 00), and to make other typographical corrections. The minimum and maximum values for the BOR trip points in Table 29-5 have changed. The new version of the table is shown below (changes in **bold**).

TABLE 29-5: BOR TRIP POINTS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial								
Param No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
DC19		BOR Voltage on VDD Transition	BOR**V** = 00	—	—	—	—	LPBOR(1)
			BOR**V** = 01	2.92	3	**3.25**	V	
			BOR**V** = 10	2.63	2.7	**2.92**	V	
			BOR**V** = 11	1.75	1.82	**2.01**	V	

Note 1: LPBOR re-arms the POR circuit, but does not cause a BOR. LPBOR can be used to ensure a POR after the supply voltage rises to a safe operating level. It does not stop code execution after the supply voltage falls below a chosen trip point.

4. Module: Product Identification System

The Product Identification System has been updated to include the MQ package option. The updated Package Information is shown below (addition in **bold**).

Architecture	24	= 16-bit modified Harvard without DSP
Flash Memory Family	F	= Flash program memory
Product Group	KA1	= General purpose microcontrollers
Pin Count	01 02	= 20-pin = 28-pin
Temperature Range	I E	= -40°C to +85°C (Industrial) = -40°C to +125°C (Extended)
Package	SP SO SS ML, **MQ** P	= SPDIP = SOIC = SSOP = QFN = PDIP
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES = Engineering Sample	

5. Module: Electrical Characteristics

The following note has been added to **Table 29-15** below (addition in **bold**).

TABLE 29-15: INTERNAL VOLTAGE REFERENCES

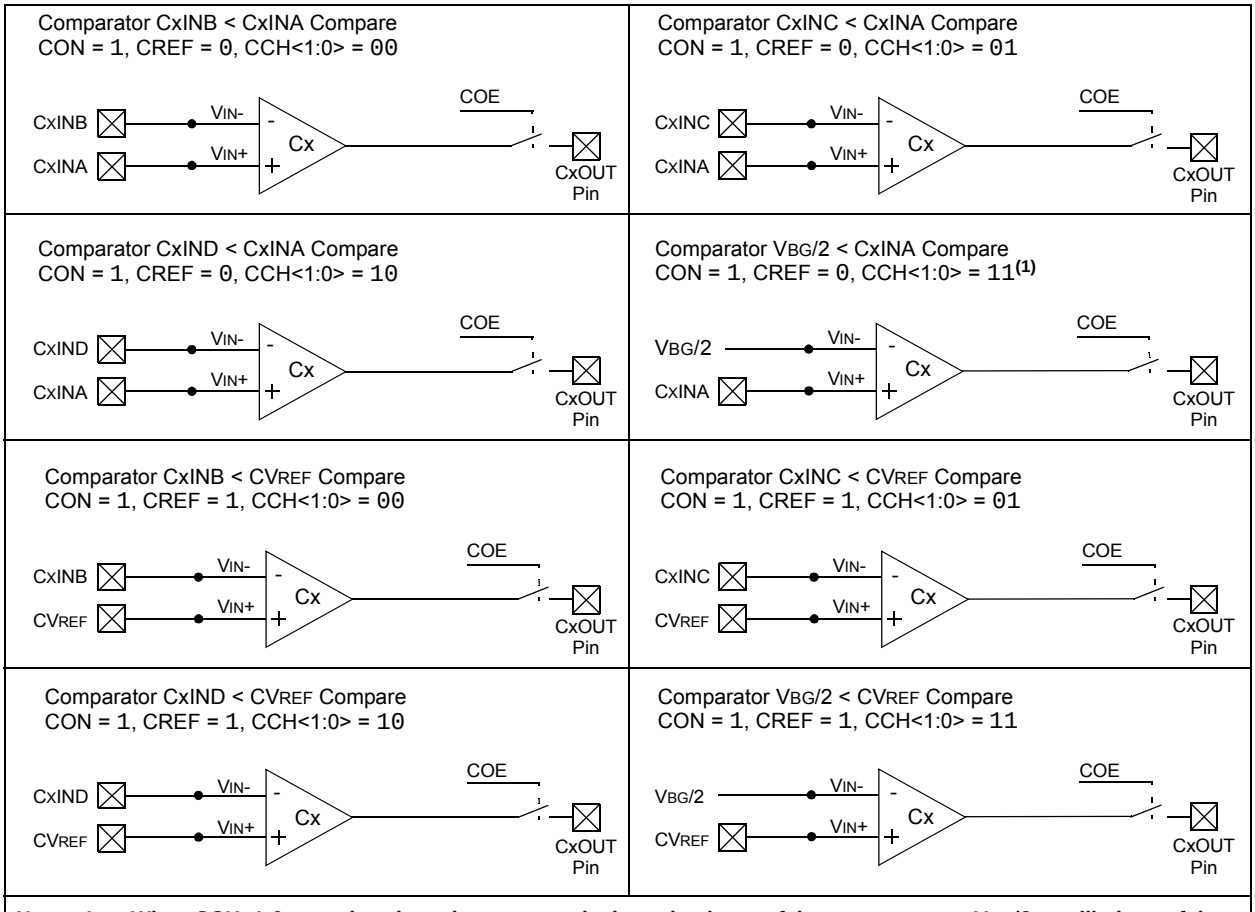
Operating Conditions: 2.0V < V_{DD} < 3.6V Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended							
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Comments
	V_{BG}	Internal Band Gap Reference	1.14	1.2	1.26	V	**Note 1**
	T_{IRVST}	Internal Reference Stabilization Time	—	200	250	µs	

Note 1: The band gap voltage (V_{BG} and $V_{BG}/2$) may oscillate while being converted through the ADC, which may result in measured values outside the data sheet specification. For a more repeatable band gap value, an average of multiple conversions is recommended.

6. Module: Comparator Module

The following note has been added to **Figure 23-2** and **Register 23-1** below (addition in **bold**).

FIGURE 23-2: INDIVIDUAL COMPARATOR CONFIGURATIONS(1)



Note 1: When CCH<1:0> = 11 is selected to connect the inverting input of the comparator to $V_{BG}/2$, oscillations of the band gap may result in unexpected results. This comparator setting (CCH<1:0> = 11) is not warranted to the data sheet specifications.

REGISTER 23-1: CMxCON: COMPARATOR x CONTROL REGISTERS

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R-0
CON	COE	CPOL	CLPWR	—	—	CEVT	COUT
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1	EVPOL0	—	CREF	—	—	CCH1(1)	CCH0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 1-0 CCH<1:0>: Comparator Channel Select bits(1)
11 = Inverting input of comparator connects to VBG/2
10 = Inverting input of comparator connects to CxIND pin
01 = Inverting input of comparator connects to CxINC pin
00 = Inverting input of comparator connects to CxINB pin

Note 1: When CCH<1:0> = 11 is selected to connect the inverting input of the comparator to VBG/2, oscillations of the band gap may result in unexpected results. This comparator setting (CCH<1:0> = 11) is not warranted to the data sheet specifications.

7. Module: Electrical Characteristics

The Min equation for TccP has been updated in Table 29-33 below (shown in **bold**).

TABLE 29-33: INPUT CAPTURE

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
IC10	TccL	ICx Input Low Time – Synchronous Timer	No Prescaler	TCY + 20	—	ns	Must also meet Parameter IC15
			With Prescaler	20	—	ns	
IC11	TccH	ICx Input Low Time – Synchronous Timer	No Prescaler	TCY + 20	—	ns	Must also meet Parameter IC15
			With Prescaler	20	—	ns	
IC15	TccP	ICx Input Period – Synchronous Timer		**2 * TCY/N + 40**	—	ns	N = prescale value (1, 4, 16)

8. Module: All Peripheral Chapters

At the beginning of all peripheral chapters, there is a note that references the *"PIC24F Family Reference Manual"* for the details of the peripheral. At the end of these notes, the following text has been added:

The information in this Data Sheet supersedes the information in the *"PIC24F Family Reference Manual"* (FRM).

9. Module: Special Features

In Register 26-9, the value for bits<15-8> **(FAMID<7:0>)** has changed (shown in **bold** below).

REGISTER 26-9: DEVID: DEVICE ID REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

R	R	R	R	R	R	R	R
FAMID7	FAMID6	FAMID5	FAMID4	FAMID3	FAMID2	FAMID1	FAMID0
bit 15							bit 8

R	R	R	R	R	R	R	R
DEV7	DEV6	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-16 Unimplemented: Read as '0'

bit 15-8 FAMID<7:0>: Device Family Identifier bits
00001101 = PIC24F16KA102 family

bit 7-0 DEV<7:0>: Individual Device Identifier bits
00000011 = PIC24F16KA102
00001010 = PIC24F08KA102
00000001 = PIC24F16KA101
00001000 = PIC24F08KA101

10. Module: Power-Saving Features

In **Register 10-4**, the bit 8 name has changed from **I2C1MD** to **IC1MD**.

11. Module: CTMU

The second paragraph in **Section 25.3 "Pulse Generation and Delay"** has been updated with the following text:

When the module is configured for pulse generation delay by setting the TGEN bit (CTMUCON<12>), the internal current source is connected to the B input of Comparator 2. A capacitor (CDELAY) is connected to the Comparator 2 pin, C2INB, and the Comparator Voltage Reference, CVREF, is connected to C2INA. CVREF is then configured for a specific trip point. The module begins to charge CDELAY when an edge event is detected. When CDELAY begins charging, CTPLS goes low and when CDELAY reaches the CVREF trip point, CTPLS goes high.

12. Module: Oscillator Configuration

The FRC Oscillator with Postscaler (LPFRCDIV) has been changed from 500 MHz to 500 kHz (shown in **bold** below).

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	Note
8 MHz FRC Oscillator with Postscaler (FRCDIV)	Internal	11	111	1, 2
500 **kHz** FRC Oscillator with Postscaler (LPFRCDIV)	Internal	11	110	1

13. Module: Flash Program Memory

The following change, shown in **bold** below, has been made to the first paragraph in **Section 5.0 "Flash Program Memory"**:

The **PIC24F16KA** family of devices contains internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable when operating with V_{DD} over 1.8V.

14. Module: Device Overview

Additional data has been added to Table 1-2 (additions shown in **bold** below).

TABLE 1-2: PIC24F16KA102 FAMILY PINOUT DESCRIPTIONS

Function	Pin Number				I/O	Input Buffer	Description
	20-Pin PDIP/SSOP/ SOIC	20-Pin QFN	28-Pin SPDIP/ SSOP/SOIC	28-Pin QFN			
U2BCLK	9	6	11	8	O	—	UART2 IrDA® Baud Clock
$\overline{U2CTS}$	**10**	**7**	**12**	**9**	**I**	**ST**	**UART2 Clear-to-Send Input**
$\overline{U2RTS}$	**6**	**6**	**11**	**8**	**O**	**—**	**UART2 Request-to-Send Output**
U2RX	**5**	**2**	**5**	**2**	**I**	**ST**	**UART2 Receive**
U2TX	**4**	**1**	**4**	**1**	**O**	**—**	**UART2 Transmit**

Legend: ST = Schmitt Trigger input buffer, ANA = Analog level input/output, I^2C™ = I^2C/SMBus input buffer

Note 1: Alternative multiplexing when the I2C1SEL Configuration bit is cleared.

15. Module: Comparator Module

In **Register 23-1**, bits 7-6, **EVPOL<1:0>**, have changed (changes shown in **bold** below).

bit 7-6 **EVPOL<1:0>: Trigger/Event/Interrupt Polarity Select bits**

11 = Trigger/event/interrupt generated on any change of the comparator output
10 = Trigger/event/interrupt generated on transition of the comparator output: High-to-low transition only.
01 = Trigger/event/interrupt generated on transition of the comparator output: Low-to-high transition only.
00 = Trigger/event/interrupt generation is disabled

16. Module: Electrical Specifications

Table 29-9 is amended to add the specification, DI57 (Input Leakage Current, OSCO/RA3). The new specification is shown below (additions in **bold**, bold in original removed for clarity).

TABLE 29-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (PARTIAL PRESENTATION)

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
	IIL	Input Leakage Current(2,3)					
DI50		I/O Ports	—	0.050	±0.100	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI51		VREF+, VREF-, AN0, AN1	—	0.300	±0.500	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI55		$\overline{\text{MCLR}}$	—	—	±5.0	µA	VSS ≤ VPIN ≤ VDD
DI56		OSCI	—	—	±5.0	µA	VSS ≤ VPIN ≤ VDD, XT and HS modes
DI57		**OSCO/RA3**	**—**	**—**	**±2.0**	**µA**	**VSS ≤ VPIN ≤ VDD**

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

17. Module: Electrical Specifications

The maximum values for specification DC61 (WDT Current, 3.3V) are corrected as shown in Table 29-8 below. Corrections are shown in **bold** (bold in original and footnotes removed for clarity).

TABLE 29-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD) (PARTIAL PRESENTATION)

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	Typical(1)	Max	Units	Conditions		
Power-Down Current (IPD): PMD Bits are Set, PMSLP Bit is '0'(2)						
DC61e	0.87	0.95	µA	-40°C	3.3V	Watchdog Timer Current: WDT(3,4)
DC61f		**1.1**		+25°C		
DC61g		**1.1**		+60°C		
DC61h		**1.2**		+85°C		
DC61i		1.5		+125°C		

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (6/2009)

Initial release of this document; issued for revision A5. Includes silicon issues 1 (CTMU), 2 (Resets – BOR), 3 (Core – ICSP), 4 (Core – Deep Sleep), 5 (Memory – Code Protection), 6 (Comparator) and 7 (SPI – Enhanced Buffer Mode). Includes data sheet clarifications 1 (Memory), 2 (Electrical Specifications – AC Specifications), 3-6 (Electrical Specifications – DC Specifications), 7 (A/D) and 8 (Comparators).

Rev B Document (6/2009)

Revision issued for silicon revision A6. Existing silicon issues 1 (CTMU), 2 (Resets – BOR), 4 (Core – Deep Sleep), 6 (Comparator) and 7 (SPI – Enhanced Buffer Mode) added to revision A6. No new issues added.

Rev C Document (10/2009)

Revision issued for silicon revision A7. Existing silicon issues 1 (CTMU), 2 (Resets – BOR), 4 (Core – Deep Sleep), 6 (Comparator) and 7 (SPI – Enhanced Buffer Mode) added to revision A7. Added new silicon issue 8 (I/O Ports – PORTA and PORTB).

To revision B of the data sheet, adds data sheet clarifications 9 (Pin Diagrams), 10 (A/D Converter – AD1CHS Register), 11 (A/D Converter – AD1CHS Register), 12 (Special Features – Configuration Bits), 13 (Power-Saving Features) and 14 (Electrical Specifications – AC Specifications).

Rev D Document (10/2009)

Typographic correction: updated Table 2 with the correct associations between silicon issues and silicon revisions.

Rev E Document (4/2010)

Added new silicon issue 9 (I/O Ports – PORTA and PORTB) to all silicon revisions.

Updated existing silicon issue 8 to include additional interactions and work arounds between RA0 and RB0.

Added data sheet clarification 15 (Electrical Specifications – DC Specifications) to revision B of the data sheet.

Updated revision history to include entry for revision D.

Rev F Document (11/2010)

Revision issued for silicon revision B0. Existing silicon issues 2 (Resets – BOR) and 6 (Comparator) added to revision B0.

Amended existing silicon issue 8 (I/O Ports – PORTA and PORTB), to change “digital input” to analog input” at the end of the fourth paragraph.

Added new silicon issue 10 (Core – Low Power BOR) to silicon revisions A5, A6 and A7.

Added new silicon issues 11, 12 (Comparator) and 13 (Core – Doze Mode) to silicon revisions A5, A6 and A7.

Removed data sheet clarification 16 (Electrical Specifications – DC Specifications) to revision B of the data sheet.

Removed data sheet clarification 6 (Electrical Specifications – DC Specifications) and combined it with data sheet clarification 16 which is now data sheet clarification 15.

Rev G Document (4/2011)

Added silicon issue 13 (A/D Converter) to silicon revisions A5, A6 and A7. Silicon issue 6 (Comparator) edited to no longer affect revision B0. Silicon issue 10 (Core – Low-Power BOR) description was edited to explicitly include the acronym, LPBOR. Silicon issue 11 (Comparator) was published in error and has been deleted. Silicon issue 12 (Comparator) work around has been shortened for clarity.

Data sheet clarification 15 (Electrical Specifications – DC Specification) has been edited to explicitly name BORV = 00 as the LPBOR. Note 1, explaining the LPBOR, explicitly differentiates BOR and LPBOR functionality.

Rev H Document (4/2012)

Added data sheet clarification 16 (Product Identification System).

Rev J Document (6/2013)

Added silicon issue 14 (HLVD (Band Gap Reference). Removed the following data sheet clarifications since they have been addressed/corrected in Revision C of the data sheet:

- 2 (Electrical Specifications – AC Specifications)
- 3 (Electrical Specifications – DC Specifications)
- 4 (Electrical Specifications – DC Specifications)
- 5 (Electrical Specifications – DC Specifications)
- 7 (Comparators)
- 8 (Pin Diagrams)
- 9 (A/D Converter – AD1CHS Register)
- 10 (A/D Converter)
- 11 (Special Features – Configuration Bits)
- 12 (Power Saving Features)
- 13 (Electrical Specifications – AC Specifications)

Rev K Document (1/2014)

Added data sheet clarifications 5 (Electrical Characteristics), 6 (Comparator Module), 7 (Electrical Characteristics, 8 (All Peripheral Chapters), 9 (Special Features), 10 (Power-Saving Features), 11 (CTMU), 12 (Oscillator Configuration), 13 (Flash Program Memory), 14 (Device Overview) and 15 (Comparator Module).

Rev L Document (4/2014)

Added data sheet clarification 16 (Electrical Specifications).

Corrects Device IDs shown in Table 1.

Rev M Document (7/2014)

Added data sheet clarification 17 (Electrical Specifications).

Rev N Document (6/2015)

Added silicon revision B1.

Rev P Document (10/2016)

Changed the DI57 Max Value in data sheet clarification 16 (Electrical Specifications) from ±1.0 µA to ±2.0 µA.

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